

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Curcio et al	)	Examiner:
	)	
Serial No.: To be assigned	)	Art Unit:
	)	
Filed: Herewith	)	
	)	
For: <b>METHOD AND STRUCTURE FOR</b>	)	
<b>PRODUCING Z-AXIS INTERCONNECTION</b>	)	
<b>ASSEMBLY OF PRINTED WIRING BOARD</b>	)	

Docket No. END920000122US1 (IEN-10-5530)

**INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being filed to fulfill the duty of candor and good faith toward the Patent and Trademark Office, as required pursuant to 37 C.F.R. § 1.56.

Listed on the attached PTO form 1449 is information known to persons substantively involved in the preparation of the application identified above, and that a reasonable Examiner would consider important when deciding whether to allow the application. This document is not to be construed as a representation that a search to locate the most relevant information has been made, nor a representation that more pertinent information does not exist.

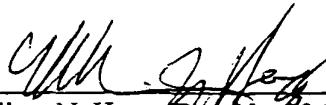
Copies of the information listed on the attached PTO Form 1449 are provided herewith.

The identification of any information herein is not intended to be, and should not be understood as being, an admission that such information, in fact, constitutes "prior art" within the meaning of applicable law. The "prior art" status of any information is a matter to be resolved during prosecution.

This Information Disclosure Statement is being filed the application. Accordingly, it is not believed that any fee is required relating to the filing of this Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 03-0172.

Respectfully submitted,

Date: 3-8-01

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enclosures

Subst. Form PTO-1449	Serial No.: To be assigned	
APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: END920000122US1 (IEN-10-5530)	
	Applicant: Curcio et al	
	Filing Date: Herewith	Group:

## U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
	AA	3,795,047	03/05/74	Abolafia et al	29	625	06/15/72
	AB	5,092,032	03/03/92	Murakimi	29	830	05/15/91
	AC	5,135,606	08/04/92	Kato et al	156	631	12/07/90
	AD	5,200,026	04/06/93	Okabe	156	651	05/15/91
	AE	5,322,593	06/21/94	Hasegawa et al	156	633	11/20/92
	AF	5,624,268	04/29/97	Maeda et al	439	66	01/17/96
	AG	5,819,406	10/13/98	Yoshizawa et al	29	877	07/30/96
	AH	5,984,691	11/16/99	Brodsky et al	439	66	03/10/98
	AI	6,059,579	05/09/00	Kresge et al	439	66	09/24/97
	AJ						
	AK						

## FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subcl.	Translation?
	AL						
	AM						
	AN						

## OTHER DOCUMENTS

	AO	U.S. Application of Appelt et al for "Manufacturing Methods for Printed Circuit Boards and Printed Circuit Boards Made Thereby", Serial No. 08/968,988 (IBM Docket EN9-97-032)
	AP	U.S. Application of Lauffer et al for "Composite Laminate Circuit Structure and Methods of Interconnecting the Same" (IBM Docket EN9-99-081)
	AQ	IBM Technical Disclosure Bulletin, Vol. 37, No. 02A, "Improved and Cost-Reduced Interposer for Higher-Risk Processes", February, 1994
	AR	"Multi Layer Substrate with Low Coefficient of Thermal Expansion", Kei Nakamura et al, 2000 International Symposium on Microelectronics, pp 235-240
	AS	
	AT	

Examiner:

Date Considered: